EXHIBIT 6

FILED UNDER SEAL

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., *Plaintiff*, v. MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., MICRON TECHNOLOGY TEXAS LLC, *Defendants*.	§ § § § § § § § § § § §	CIVIL ACTION NO. 2:22-CV-00203-JRG-RSP

CLAIM CONSTRUCTION ORDER

Netlist, Inc., asserts claims from six patents relating to computer memory against Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC (together, "Micron"). U.S. Patent 10,949,339, entitled "Memory Module with Controlled Byte-Wise Buffers," relates to improving the performance and memory capacity of memory subsystems. '339 Patent at 1:18–23. U.S. Patent 10,860,506, entitled "Memory Module With Timing-Controlled Data Buffering," generally concerns "multi-rank memory modules and methods of operation." '506 Patent at 1:37–39. U.S. Patents 11,016,918 and 11,232,054, which are related and share a common specification, concern computer memory devices that use different types of memory. '918 Patent at 1:66–2:2; *see also* '054 Patent at 1:66–2:2. Finally, U.S. Patents 8,787,060 and 9,318,160, which are related and share a common specification, concern "systems and methods for reducing the load of drivers of memory packages included on memory modules." '060 Patent at 1:19–21; *see also* '160 Patent at 1:21–23.

The parties dispute the proper constructions of 17 terms from the patents, six of which were previously construed by this Court in *Netlist v. Samsung*, No. 2:21-CV-00463-JRG (*Samsung I*). *See generally* Cl. Constr. Order, Dkt. No. 98-7. Having considered the parties' briefing, along with arguments of counsel during a July 26, 2023 hearing, the Court resolves the disputes as follows.

I. LEGAL STANDARDS

A. Generally

"'[T]he claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Innova/Pure-Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). As such, if the parties dispute the scope of the claims, the court must determine their meaning. *See, e.g.*, *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1317 (Fed. Cir. 2007); *see also Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 390 (1996), *aff'g*, 52 F.3d 967, 976 (Fed. Cir. 1995) (en banc).

Claim construction, however, "is not an obligatory exercise in redundancy." *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997). Rather, "[c]laim construction is a matter of [resolving] disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims . . . ." *Id.* A court need not "repeat or restate every claim term in order to comply with the ruling that claim construction is for the court." *Id.*

When construing claims, "[t]here is a heavy presumption that claim terms are to be given their ordinary and customary meaning." *Aventis Pharm. Inc. v. Amino Chems. Ltd.*, 715 F.3d 1363, 1373 (Fed. Cir. 2013) (citing *Phillips*, 415 F.3d at 1312–13). Courts must therefore "look to the words of the claims themselves . . . to define the scope of the patented invention." *Id.* (citations omitted). "[T]he ordinary and customary meaning of a claim term is the meaning that the term

would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Phillips*, 415 F.3d at 1313. This "person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Id.*

Intrinsic evidence is the primary resource for claim construction. *See Power-One, Inc. v. Artesyn Techs., Inc.*, 599 F.3d 1343, 1348 (Fed. Cir. 2010) (citing *Phillips*, 415 F.3d at 1312). For certain claim terms, "the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words." *Phillips*, 415 F.3d at 1314; *see also Medrad, Inc. v. MRI Devices Corp.*, 401 F.3d 1313, 1319 (Fed. Cir. 2005) ("We cannot look at the ordinary meaning of the term . . . in a vacuum. Rather, we must look at the ordinary meaning in the context of the written description and the prosecution history."). But for claim terms with less-apparent meanings, courts consider "'those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean[,] [including] the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art.'" *Phillips*, 415 F.3d at 1314 (quoting *Innova*, 381 F.3d at 1116).

B. Means-Plus-Function Claiming

A patent claim may be expressed using functional language. *See* 35 U.S.C. § 112 ¶ 6 (pre-AIA); *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1347–49 & n.3 (Fed. Cir. 2015) (en banc in relevant portion). Under 35 U.S.C. § 112 ¶ 6, a structure may be claimed as a "means . . . for

performing a specified function," and an act may be claimed as a "step for performing a specified function." *Masco Corp. v. United States*, 303 F.3d 1316, 1326 (Fed. Cir. 2002). When it applies, § 112 ¶ 6 limits the scope of the functional term "to only the structure, materials, or acts described in the specification as corresponding to the claimed function and equivalents thereof." *Williamson*, 792 F.3d at 1347.

But § 112 ¶ 6 does not apply to all functional claim language. There is a rebuttable presumption that § 112 ¶ 6 applies when the claim language includes "means" or "step for" terms, and a rebuttable presumption it does *not* apply in the absence of those terms. *Masco Corp.*, 303 F.3d at 1326; *Williamson*, 792 F.3d at 1348. These presumptions stand or fall according to whether one of ordinary skill in the art would understand the claim with the functional language, in the context of the entire specification, to denote sufficiently definite structure or acts for performing the function. *See Media Rights Techs., Inc. v. Capital One Fin. Corp.*, 800 F.3d 1366, 1372 (Fed. Cir. 2015) (noting § 112 ¶ 6 does not apply when "the claim language, read in light of the specification, recites sufficiently definite structure" (quotation marks omitted) (citing *Williamson*, 792 F.3d at 1349; *Robert Bosch, LLC v. Snap-On Inc.*, 769 F.3d 1094, 1099 (Fed. Cir. 2014))); *Williamson*, 792 F.3d at 1349 (noting § 112 ¶ 6 does not apply when "the words of the claim are understood by persons of ordinary skill in the art to have sufficiently definite meaning as the name for structure"); *Masco Corp.*, 303 F.3d at 1326 (noting § 112 ¶ 6 does not apply when the claim includes an "act" corresponding to "how the function is performed"); *Personalized Media Commc'ns, LLC v. I.T.C.*, 161 F.3d 696, 704 (Fed. Cir. 1998) (noting § 112 ¶ 6 does not apply when the claim includes "sufficient structure, material, or acts within the claim itself to perform entirely the recited function . . . even if the claim uses the term 'means.'" (quotation marks and citation

omitted)). *See also Williamson*, 792 F.3d at 1350 (noting "'[m]odule' is a well-known nonce word that can operate as a substitute for 'means' in the context of § 112, para. 6").

C. Indefiniteness

"[A] patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc*., 572 U.S. 898, 901 (2014). The claims "must be precise enough to afford clear notice of what is claimed," but that consideration must be made while accounting for the inherent limitations of language. *Id.* at 908.

"Indefiniteness must be proven by clear and convincing evidence." *Sonix Tech. Co. v. Publ'ns Int'l, Ltd.*, 844 F.3d 1370, 1377 (Fed. Cir. 2017). And in the context of § 112 ¶ 6, "[t]he party alleging that the specification fails to disclose sufficient corresponding structure must make that showing by clear and convincing evidence." *TecSec, Inc. v. IBM*, 731 F.3d 1336, 1349 (Fed. Cir. 2013) (quoting *Budde v. Harley-Davidson, Inc*., 250 F.3d 1369, 1380–81 (Fed. Cir. 2001)).

II. THE LEVEL OF ORDINARY SKILL IN THE ART

The level of ordinary skill in the art is the skill level of a hypothetical person who is presumed to have known the relevant art at the time of the invention. *In re GPAC*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). In resolving the appropriate level of ordinary skill, courts consider the types of and solutions to problems encountered in the art, the speed of innovation, the sophistication of the technology, and the education of workers active in the field. *Id.* Importantly, "[a] person of ordinary skill in the art is also a person of ordinary creativity, not an automaton." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007).

Here, neither party proffers a level of ordinary skill in the art in its briefing. Micron's expert, however, asserts:

> a POSITA in the field of the '060 and '160 patents at the time of the claimed inventions . . . would have had . . . an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field.

Stone Decl., Dkt. No. 97-9 ¶ 23. He asserts an identical skill level for the '918 and '054 Patents. *Id.* ¶ 25. In a decision concerning a patent related to the '506 Patent, the PTAB used a modified version of this skill level, which the Court now adopts: "a person of ordinary skill in the art would have been a person with an advanced degree in electrical or computer engineering and two years working in the field, or a bachelor's degree in such engineering disciplines and three years working in the field." *See* Final Written Decision (IPR2022-00236), Dkt. No. 109-7 at 8.

III. U.S. PATENTS 8,787,060 AND 9,318,160

These related patents concern "systems and methods for reducing the load of drivers of memory packages included on memory modules." '060 Patent at 1:19–21. They describe prior-art memory devices in which one driver drives signals along a die interconnect connected to all array dies[1] of the device. *See id.* at 1:30–2:15. If the control die includes multiple drivers, each of those drivers is connected to all array dies of the device. *See id.* at fig.1B (showing drivers 184, 186 each connected to all four array dies 160).

[1] Generally, an array die is an array of memory circuits in a single piece of silicon.

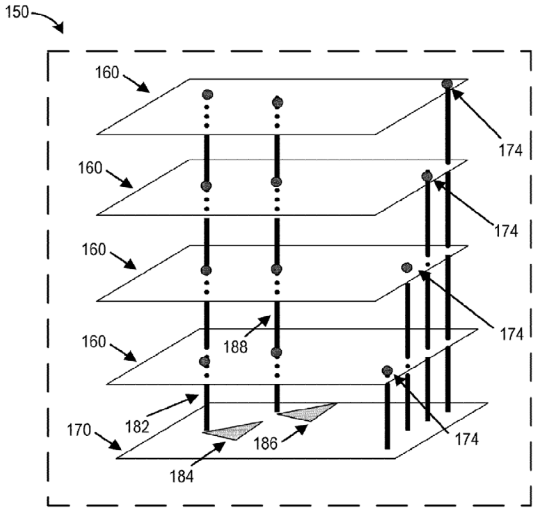

FIG. 1B

These patents address that problem by connecting a driver to less than all the array dies in a package. For example, in Figure 2 (below), one driver is connected to a data conduit 232a that interconnects only with array dies 210a, 210b. A different driver is connected to data conduit 232b, which connects only with array dies 210c, 210d.

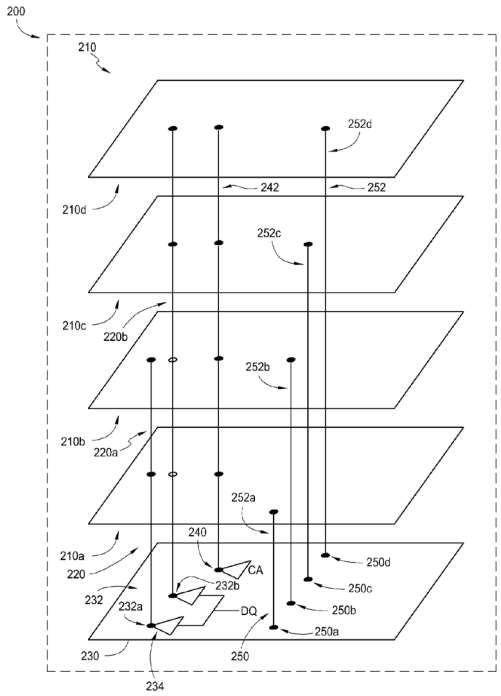

FIG. 2

The parties have three disputes concerning these two patents. First, they dispute the scope of "electrical communication" in the claims of both patents. Second, they dispute whether "driver size" in Claim 1 of the '160 Patent refers to a physical size or to electrical strength. Finally, Micron challenges Claim 7 of the '060 Patent as an indefinite mixed-class claim.

A. "electrical communication" ('060 Patent, Claims 1, 11, 20, 29; '160 Patent, Claim 1)

Netlist's Construction	Micron's Construction
Plain and ordinary meaning, that is, "electrical communication" is different from "electrical connection"	Plain and ordinary meaning, i.e., does not require importing "data ports" limitation into the claim to require electrical communications (or lack of electrical communications) between the die interconnect(s) and the data ports of the array die(s).

The relevant claims generally recite first die interconnects in "electrical communication" with a first group of array dies, and second die interconnects in "electrical communication" with a second group of array dies. For example, the third limitation of Claim 1 of the '060 Patent recites:

> at least a first die interconnect and a second die interconnect, the first die interconnect in *electrical communication* with the first group of array dies and not in *electrical communication* with the second group of at least one array die, the second die interconnect in *electrical communication* with the second group of at least one array die and not in *electrical communication* with the first group of array dies[.]

'060 Patent at 23:65–24:5 (emphasis added); see also '160 Patent at 23:51–58.

The parties present two disputes about "electrical communication." First, according to Netlist, "an 'electrical *connection*' may exist without resulting in any 'electrical *communication*' between the die interconnect(s) and array die(s) by not 'provid[ing] electrical communication with the memory cells of the array die.'" Dkt. No. 97 at 3 (quoting '060 Patent at 8:53–62). Or put

another way, "a die is 'not in electrical communication' when it is not responsive to the data signal being transmitted by the die interconnect.'" *Id.* (quoting '060 Patent at 8:42–44).

Micron agrees "electrical communication" and "electrical connection" "have somewhat different and somewhat overlapping meanings," Dkt. No. 109 at 2, but does not elaborate on that position. Instead, Micron focuses on whether "electrical communication" requires importing limitations of "data ports" or "responsiveness." *Id.* It suggests Netlist previously argued (in *Samsung I*) the claim should be interpreted to mean "electrical communication with the data ports of the group of array dies." *Id.* at 2. It also notes Netlist's opening position that "a die is 'not in electrical communication' when it is not responsive to the data signal being transmitted by the die interconnect.'"[2] *Id.* (quoting Dkt. No. 97 at 3).

Netlist replies that, despite Micron's apparent agreement these terms have different scope, Micron's expert testified otherwise. Dkt. No. 110 at 1. Netlist also stresses it treated a die interconnect as in "electrical communication" with an array die even when the array die's data port was disabled, and thus without regard to "responsiveness." *See* Dkt. No. 110 at 2.

1. The scope of "electrical communication" and "electrical connection"

The specification makes clear that these terms have different scope. For one, electrical communication must be "enabled" and may be "prevented":

> [T]he die interconnects 220 may use via holes to pass through an array die that is not configured to be in electrical communication with the die interconnect. For instance, die interconnect 220b may pass through array dies 210a and 210b using TSVs that do not *enable electrical communication* between the die interconnect 220b and data ports of the array dies 210a and 210b . . . . In cases where the die interconnect passes through an array die that is not configured to be in electrical

[2] Micron's original construction did not reference "responsiveness." It added "or responsiveness" to its proposed construction based on Netlist's opening brief. *See* Dkt. No. 109 at 2 n.2.

> communication with the die interconnect, the TSV may include an insulator or an air gap between the die interconnect and the array die circuitry that is large enough to *prevent electrical communication* between the die interconnect and the array die circuitry. . . .

'060 Patent at 8:35–33 (emphasis added); *see also id.* at 5:41–45 ("Each of the array die 210 may include one or more data ports . . . . The data ports *enable* electrical communication and data transfer between the corresponding memory circuitry of the array dies 210 and a communication path way (e.g., a die interconnect)." (emphasis added)). Similarly, the specification expressly distinguishes between "electrical connections" and electrical communication, explaining

> *electrical connections* leading from the TSV of the array dies that are not configured to be in *electrical communication* with the die interconnect may not exist or may be stubs. These stubs are not configured to provide *electrical communication* with the memory cells of the array die.

'060 Patent at 8:57–63 (emphasis added). All of these uses of "communication" comport with the ordinary meaning of the term as an act. *See, e.g., communication*, https://www.yourdictionary.com/communication ("[t]he act of transmitting"; "a giving or exchanging of information, signals, or messages as by talk, gestures, or writing").

Micron makes no real argument in opposition, but simply claims "Netlist has not identified any reason" for the Court to construe the claim. Dkt. No. 109 at 2. But given the testimony of Micron's expert, *see* Dkt. No. 110 at 1,[3] a dispute about scope exists and must be resolved. Considering the specification's use of the term, the Court agrees the plain and ordinary meaning of "electrical communication" is different from "electrical connection."

[3] *Samsung I* Trial Tr., Dkt. No. 110-2 at 95 ("Is it your testimony that the connection between a TSV and a stub is electrical communication? A. Yeah. This demonstrates it, because the wave travels on that. Q. Okay. What does the word "electrical communication" mean to you? A. Electrical connection. That's -- I got that from the patent. I can show you where he says that.").

2. The alleged importation by Netlist of "data port" and "responsiveness"

Concerning "data ports," Micron points to Netlist's trial argument during *Samsung I* that, "if it doesn't hook up to the data port, it means there is no electrical communication; whereas, above that, if there is a data port present, then we will have that electrical communication." Dkt. No. 109 at 2 (quoting Samsung *I* Trial Tr., Dkt. No. 109-2 at 314:13–17). Although Micron argues this is an attempt to import a "data port" limitation into the claims, considered in the proper context, this is simply an infringement argument by Netlist rather than a dispute about scope. That said, if Netlist's position is the mere presence of "data ports" is enough to meet the "electrical communication" requirement for the purpose of determining infringement or invalidity, the Court agrees with Micron that is improper.

Regarding "responsiveness," Netlist appears to agree that responsiveness is not required for electrical communication. Specifically, it notes its prior position that "signals received by the input stage of the receiver" are sufficient to meet the limitation, without regard to responsiveness. *See* Dkt. No. 110 at 2. Accordingly, the Court sees no dispute to resolve.

Based on the foregoing, the Court agrees with Netlist that "electrical communication" is different from "electrical connection." The Court also agrees with Micron that the existence of data ports, without more, does not satisfy the "electrical communication" requirement in the claims. With this guidance, however, the Court will give this term a "plain and ordinary meaning" construction.

B. "the second driver size being different from the first driver size" ('160 Patent, Claim 1)

Netlist's Construction	Micron's Construction
Plain and ordinary meaning, that is, "the size of the second driver being different from the size of the first driver"	"the physical dimensions of the second driver being different from the physical dimensions of the first driver"

Claim 1 recites "first drivers each having a first driver size," "second drivers each having a second driver size," and "the second driver size being different from the first driver size." '160 Patent at 23:62–24:3. The parties dispute whether "driver size" refers to the physical dimensions of the driver or its "strength."

Collectively, the parties point to the following excerpts from the patents:

- "The size of the driver may be adjusted by the selection of the transistor size and/or number of transistors included in the driver." '160 Patent at 17:31–33.
- "Generally, a load exists on each of the drivers 134, 140, 184, and 186 by virtue of the drivers being in electrical communication with the corresponding die interconnects and the corresponding circuitry of the array dies. Thus, *to drive a signal along a die interconnect, a driver typically must be large enough to overcome the load on the driver. However, generally a larger driver not only consumes more space on the control die, but also consumes more power.*" *Id.* at 2:10–17 (emphasis added).
- "[C]ertain embodiments of the present disclosure enable a reduction in the load of the conduits 332. Consequently, in some embodiments, *the drivers 334 may each be smaller than a single driver that is configured to drive a signal from a conduit along a single die interconnect that is in electrical communication with a port from each of the array dies 310. Moreover, the drivers 334 may include smaller transistor sizes than a single driver that is configured to drive a signal to each of the array dies 110.*" *Id.* at 13:13–26.

Micron also proffers the declaration of its expert, who explains "driver size and driver strength are distinct engineering concepts." Stone Decl., Dkt. No. 97-9 ¶ 44.

The Court agrees "size" refers to physical dimensions. Micron presents unrebutted expert testimony on that point. Netlist, on the other hand, presents no argument that "driver size" refers to something other than physical dimensions, but instead asks a series of hypothetical questions about Micron's proposed construction. *See* Dkt. No. 97 at 4. Third, the specification links driver size to physical dimensions. '160 Patent at 2:10–17 (noting that "to drive a signal along a die interconnect, a driver typically must be large enough to overcome the load on the driver. However, generally a larger driver not only consumes more space on the control die, but also consumes more power.").

Netlist's best "evidence" appears to be Micron's argument in an IPR proceeding that "a POSITA would have been motivated by Wyman . . . to use drivers of different strengths (i.e., 'first drivers' having a 'first driver size' and 'second drivers' having a 'second driver size') . . . ." Dkt. No. 97 at 4 (quoting Petition, Dkt. No. 97-12 at 48). Netlist then cites the pre-IPR case *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1330 (Fed. Cir. 2003), for the proposition that "claims are construed the same way for both validity and infringement" *Id.* The Court agrees, but Netlist cites no authority preventing an accused infringer from making one argument before the PTAB and another before a district court. Regardless, even in the Petition, Micron distinguishes between driver size and driver strength. *See* Petition, Dkt. No. 97-12 at 48–49 (citing to EX1030 as "disclosing different-sized transistors to achieve different driver strengths"). Because the weight of the evidence supports Micron's position, the Court construes "driver size" as "driver physical size."

C. Indefiniteness of Claim 7 of the '060 Patent as Mixed-Class Claim

Claim 7, which depends from Claim 1, recites:

> wherein a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are selected in consideration of a load of the first die interconnect and a load of the second die interconnect so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit . . . .

'060 Patent at 24:37–47. Relying on *IPXL Holdings, LLC v. Amazon.com, Inc.*, 430 F.3d 1377 (Fed. Cir. 2005), Micron argues this term is "broad enough to encompass a user selecting array dies in consideration of the recited loads." Dkt. No. 109 at 5. Moreover, says Micron, "the specification is replete with examples of programming memory modules in various ways." *Id.* (citing '060 Patent at 19:13–14, 18:67–19:1, 22:28, 23:33–45). Micron stresses the language in question "contains no indication whether the array die are selected during manufacturing or when programming the memory module to operate in various ways." *Id.* at 6.

In *IPXL Holdings*, Claim 1 recited "[a]n electronic financial transaction system" comprising "an input mechanism for providing input to a processor." *IPXL Holdings*, 430 F.3d at 1384. Claim 25, which indirectly depended from Claim 1, recited "the user uses the input [mechanism] to either change the predicted transaction information or accept the displayed transaction type and transaction parameters." *Id.* The court concluded "that, as a result of the combination of two separate statutory classes of invention, a manufacturer or seller of the claimed apparatus would not know from the claim whether it might also be liable for contributory infringement because a buyer or user of the apparatus later performs the claimed method of using the apparatus." *Id.* That conclusion "was based on the lack of clarity as to when the mixed subject matter claim would be infringed." *Microprocessor Enhancement Corp. v. Texas Instruments Inc.*, 520 F.3d 1367, 1374 (Fed. Cir. 2008).

Two other often-cited cases address the same issue—*In re Katz Interactive Call Processing Patent Litig.*, 639 F.3d 1303 (Fed. Cir. 2011), and *H-W Tech., L.C. v. Overstock.com, Inc.*, 758 F.3d 1329 (Fed. Cir. 2014). In *In re Katz*, Judge Bryson wrote:

> Claims 1, 2, and 83 of the [patent at issue] cover a system with an "interface means for providing automated voice messages . . . to certain of said individual callers, wherein said certain of said individual callers digitally enter data." The district court found "no meaningful distinction" between those claims and the claim at issue in *IPXL.*
>
> Katz seeks to distinguish *IPXL* on the ground that the term "wherein" does not signify a method step but instead defines a functional capability. We disagree and uphold the district court's ruling. Like the language used in the claim at issue in *IPXL* ("wherein . . . the user uses"), the language used in Katz's claims ("wherein . . . callers digitally enter data" and "wherein . . . callers provide . . . data") is directed to user actions, not system capabilities.

In re Katz, 639 F.3d at 1318. As in *IPXL*, the claim language was written in active voice such that there was no question about who was using (the user), entering data (callers), or providing data (callers).

The patent at issue in *H-W Technology* recited "[a] tangible computer readable medium encoded with computer program . . . comprising the steps of:"

> wherein *said user completes a transaction* with at least one of said merchants listed without the need to generate a voice call;
>
> wherein said information received by said user comprises a variety of offers, wherein *said user selects* one of said variety of offers associated with said one of said merchants listed, wherein said selected offer is transmitted to said one of said merchants listed electronically . . . .

H-W Tech., 758 F.3d at 1335 (emphasis added). The court concluded "the disputed language ('wherein said user completes . . .' and 'wherein said user selects . . .') is nearly identical to the

disputed language in [*IPXL* and *In re Katz*]. And, as in those cases, it is unclear here when infringement would occur." *Id.* at 1336 (holding the claim indefinite).

The Court sees no such lack of clarity here, and holds the claim is not indefinite as a mixed-class claim. The claim is clearly directed to a "memory package" and, unlike the language in *IPXL*, *In re Katz*, and *H-W Technology*, the claim does not introduce the notion of a "user." While the passive-voice nature of the "selected" language might be grammatically broad enough to cover selection by a person, Micron proffers no reason, nor can the Court imagine, why a skilled artisan would read an apparatus claim that way.

IV. U.S. PATENT 10,860,506

A. "one or more previous operations" ('506 Patent, Claims 1–3, 11, 15, 16)

Netlist's Construction	Micron's Construction
"one or more previous memory operations"	"one or more previous memory operations" where "memory operations" are different from "leveling operations"

The parties agree that "one or more previous operations" in these claims means "one or more previous memory operations." Dkt. No. 97 at 7; Dkt. No. 109 at 6. They disagree, however, as to whether "memory operations" includes "leveling operations," which are operations that

> adjust a write timing or a read timing in consideration of a propagation time of a signal. For example, in a write operation, "[b]ecause it takes a certain amount of propagation time until the data strobe signal DQS reaches the memory chip 200, input timings of the clock signal CK and the data strobe signal DQS are not always the same on the memory chip 200 side. To compensate for that, [a] write leveling circuit [may change] an output timing of the data strobe signal DQS. . . . [R]ead leveling operation also adjusts signal timing for a read operation.

Final Written Decision (IPR2022-00236), Dkt. No. 109-7 at 13–14 (citing and quoting U.S. Published Appl'n 2010/0312925A1 (Osanai); citations omitted).

Contending "leveling operations" are not included in "memory operations," Micron argues prosecution-history disavowal. Specifically, Micron points to Netlist's arguments in IPR2022-00236 for U.S Patent 9,824,035, which shares a common disclosure with the '506 Patent. Dkt. No. 109 at 6–7; *see also* '506 Patent at [63] (noting the patent is a "grandchild" of the '035 Patent). Netlist argues the scope of any disclaimer is limited to a specific write-leveling technique discussed in a certain standard. Dkt. No. 97 at 8.

Since Netlist filed its opening brief, the PTAB issued its Final Written Decision, which recaps the entire proceeding nicely. The term at issue was "obtain timing information based on one or more signals received by each respective buffer circuit during a second memory operation prior to the first memory operation." *See* Final Written Decision, Dkt. No. 109-7 at 19. Micron argued the combination of two references, Osanai and Tokuhiro teach this limitation. *Id.* More specifically, Micron relied on Tokuhiro's disclosure of a delay unit that obtains a first delay time during a write leveling operation to meet the "second memory operation" and its calculation of a second delay time used for a read operation as the "first memory operation." *Id.*

In response, Netlist argued Tokuhiro's write-leveling function does not teach the recited "second memory operation" because during that function, no memory operations can be performed at all. *Id.* at 21. Netlist essentially argued Tokuhiro does not disclose memory operation because, during the write-leveling process of Tokuhiro, no commands instruct the memory to do anything at all. *Id.* at 28. That is, none of the commands that are issued during write leveling mode are "memory operations" under a plain and ordinary meaning of the term. *Id.*

The Board rejected this argument, concluding Tokuhiro's write-leveling function discloses the "second memory operation." The Board reasoned "the '035 Patent describes memory operations fairly broadly." *Id.* at 31 (citing '035 Patent at 3:27–32 ("[t]he memory module is

operable to perform memory operations in response to memory commands (e.g. read, write, refresh, precharge, etc.), each of which is represented by a set of control/address (C/A) signals transmitted by the memory controller to the memory module"). Moreover, the Board called Netlist's argument largely conclusory and noted it only referred back to arguments showing that no *other* memory operations are performed during write leveling rather than showing write leveling *itself* is not a memory operation. *Id.* at 33.

While this background is helpful, most importantly the Board rejected the allegedly disclaiming position. And although neither party cites authority for the proposition that for a statement to be disclaimer the patent must be granted (in the context of examination) or maintained (in the context of an IPR), Netlist takes that position and Micron implicitly agrees). *See* Dkt. No. 110 at 4 ("The Board did not agree with Netlist that write leveling is not a memory operation."); Micron's Proposed Constructions & Identification of Supporting Evid., Dkt. No. 69-2 at 4 ("Micron is making this argument only to the extent that Netlist is successful in IPR2022-00236 or IPR2023-00205 where Netlist argued that level is not a memory operation."); Dkt. No. 109 at 7 n.3 (noting the PTAB issued its final written decision after Netlist filed its opening brief, Netlist has not indicated whether it will appeal, and the resolution of any appeal may impact claim construction in this proceeding). Thus, because the allegedly disclaiming statements did not maintain the claim at issue, the Court concludes there is no disclaimer. *See Aylus Networks, Inc. v. Apple Inc.*, 856 F.3d 1353, 1360 ("Extending the prosecution disclaimer doctrine to IPR proceedings will ensure that claims are not argued one way in order to maintain their patentability and in a different way against accused infringers."). Otherwise, the Court adopts the language agreed to by the parties: "one or more previous memory operations."

B. "determining" ('506 Patent, Claim 14)

Netlist's Construction	Micron's Construction
The step of "determining the first predetermined amount based as least on signals received by the first data buffer" occurs before the earlier recited step of "receiving . . . input C/A signals"	"during one or more previous memory operations, determining the first predetermined amount based at least on signals received by the first data buffer" where "memory operations" are different from leveling operations

This is another "IPR prosecution statement" dispute that depends on similar language from the last limitations of Claim 1 and Claim 14:

Claim 1	Claim 14
"wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations" ('506 Patent at 19:53–55)	"before receiving the input C/A signals corresponding to the memory read operation at the module control device, determining the first predetermined amount based at least on signals received by the first data buffer" ('506 Patent at 22:11–15)

Micron points to two statements from Netlist's IPR papers in which Netlist allegedly equates the two limitations. First, Netlist wrote:

> Petitioner has not made a prima facie case that Hiraishi discloses . . . "the first predetermined amount is determined based at least on signals received by the first data buffer *during one or more previous operations*," as required by independent claim 1 (referred to herein as the "strobe delay feature"). *The same deficiency exists with respect to the method of claim 14, which also recites the strobe delay feature* as follows: "delaying the first read strobe by a first predetermined amount to generate a first delayed read strobe," and "before receiving the input C/A signals corresponding to the memory read operation at the module control device, determining the first predetermined amount based at least on signals received by the first data buffer."

Dkt. No. 109 at 9 (quoting Patent Owner Prelim. Resp., Dkt. No. 109-13 at 30; emphasis by Micron). Second, Netlist wrote:

> Petitioner has failed to show that Hiraishi teaches or suggests the strobe delay feature—specifically that "the first predetermined amount [of delay to the read strobe] is determined based at least on signals received by the first data buffer *during one or more previous operations*," as recited in claim 1 *and reflected in the limitations of claim 14*.

Id. (quoting Patent Owner Resp., Dkt. No. 109-12 at 32; emphasis by Micron). Thus, Netlist clearly characterized the language of both claims as a "strobe delay feature" not taught by Hiraishi.

Importantly, however, Netlist's arguments were not based on the specific signal timing recited in either Claim, but whether Hiraishi had any "strobe delay feature" at all, regardless of timing. For example, Netlist argued the delay circuit allegedly disclosing the "strobe delay feature"

> is a circuit that is not disclosed as connected to any circuitry capable of providing any input that could alter the amount of delay applied by circuit 372 to the DQS received from the selector 332. Hence, . . . a POSITA would understand from Hiraishi's disclosure that the delay circuit 372 applies a fixed phase shift, *instead of a delay based on signals received by the buffer during a previous operation*.

Patent Owner Prelim. Resp., Dkt. No. 109-13 at 32–33 (emphasis added). Similarly, in its response under the heading "Hiraishi's Read Leveling Circuit Does Not Control the Delay Circuit," Netlist stated:

> the delay applied by Hiraishi's delay circuit 372 is fixed and is not controllable by the data register control circuit 320, and Hiraishi does not disclose any other control circuit in data buffer 300 . . . . As such, the *Petitioner has failed to show that Hiraishi teaches or suggests the strobe delay feature*—specifically that "the first predetermined amount [of delay to the read strobe] is determined based at least on signals received by the first data buffer during one or more previous operations," as recited in claim 1 and reflected in the limitations of claim 14.

Patent Owner Resp., Dkt. No. 109-12 at 32 (emphasis added; brackets in original). And at least according to Netlist, even Samsung did not suggest any material differences between Claim 1 and Claim 14. *Id.* at 32 n.5.

Because making distinctions between the scope of the limitations in question was not necessary to respond to Samsung's argument, Netlist treated the limitations as similar for brevity, which does not give rise to disclaimer on this record. Given that resolves the dispute, the Court will give this term a "plain and ordinary meaning" construction.

V. U.S. PATENT 10,949,339

A. Background

According to the '339 Patent, designing memory subsystems requires balancing memory density, power dissipation, speed, and cost. '339 Patent at 2:5–7. Adjusting one of these may negatively affect the others. *Id.* at 2:7–12. For example, the '339 Patent notes two ways of increasing memory space: (1) an address decoding scheme, and (2) combining chip-select and address signals "to increase the number of physically addressable memory spaces . . . ." *Id.* at 5: 15–25. But because both solutions add memory chips, the system outputs have a heavier load. That, in turn, slows the system and increases the necessary power. *Id.* at 4:27–33. Moreover, it results in uneven propagation delay, which can negatively affect internal timing of accessing memory. *Id.* at 4:38–44. As examples, Figures 1–2 show prior-art systems in which differences in trace lengths or complexity of the memory controllers affect system speed.

As shown in Figure 3A (below), the '339 Patent teaches arranging the memory devices 412 in multiple ranks A, B, C, D, and a module controller 430 configured to receive and register input control signals from a memory controller 420. The address and control signals select one of the multiple ranks to perform a read or write operation. In response, the module controller 430 outputs

a set of control signals that drive data signals between the memory controller 420 and the selected rank.

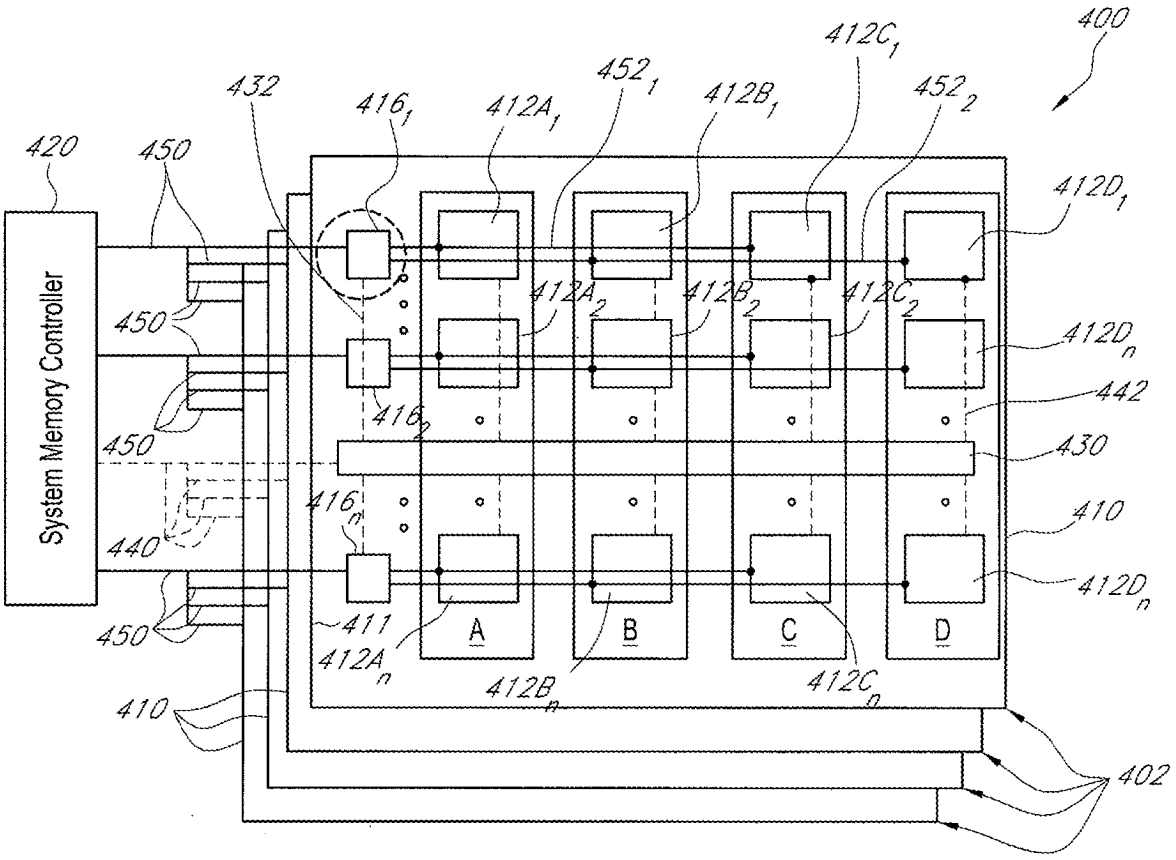

FIG. 3A

Based on signals received from the control circuit 430, the data transmission circuits 416 selectively enable or disable access to the memory devices 412. For example, whereas a set of control signals from the memory controller 420 may address two memory devices (e.g., 412A$_1$ and 412B$_1$), only one of those devices might be enabled depending on the state of the associated data transmission circuit 416$_1$. In FIG. 3A, the data transmission circuit 416$_1$ enables or disables memory devices 412A$_1$ and 412C$_1$ together and memory devices 412B$_1$ and 412D$_1$ together. *See generally* '339 Patent at 8:16–53.

B. The "drive" terms ('339 Patent, Claims 1, 11, 19, 27)

Netlist's Construction	Micron's Construction
to "drive" means "enabling only one of the data paths while the other possible paths are disabled" (i.e., no further construction necessary)	Adopts and applies the Court's adoption of the "fork- in-the-road" configuration and rejection of the "straight-line" configuration to construe "drive" to mean "enabling only one of the data paths while the other possible paths are disabled," i.e., "enable only one of the data paths for the respective byte-wise section of the N-bit wide write data while the other possible data paths for the same respective byte-wise section of the N-bit wide write data are disabled"

Claim 1 recites a module controller and a plurality of byte-wise buffers, each of which has a first side connected to data lines and a second side connected to physical memory. '339 Patent at 19:40–52; *see also id.* at 21:66–22:5 (Claim 11); *id.* at 24:18–29 (Claim 19); *id.* at 26:17–26 (Claim 27). The claims also require logic configurable to enable a data path to "actively drive" or "drive" write data from one side of the buffer to the other side:

Claim 1	"to actively drive a respective byte-wise section of the N-bit wide write data" ('339 Patent at 19:58–61)
Claim 11	"to actively drive a respective section of the N-bit wide write data" ('339 Patent at 22:2–3)
Claim 19	"to actively drive a respective section of the [first/second] N-bit wide data" ('339 Patent at 24:20–28)
Claim 27	"to drive the respective n-bit section of the write data" ('339 Patent at 26:8–9)

In *Samsung I*, Netlist argued these "drive" terms should be given a "plain and ordinary meaning" construction, whereas Samsung proposed a construction based on the fifth limitation of

Claim 1 that it called a "fork in the road" approach. *See* Cl. Constr. Order, Dkt. No. 97-8 at 7. Ultimately, the Court adopted that approach based on the specification and the prosecution history:

> A skilled artisan would understand "driving" data from one side of the buffer to the other means, when there are multiple paths in a buffer through which that data can be driven, enabling only one of the data paths while the other possible paths are disabled. Thus, "to drive" as used in these claims means "enabling only one of the data paths while the other possible paths are disabled."

Id. at 10.

Here, Netlist proposes the same construction, while Micron proposes modifying the construction to "enable only one of the data paths for the respective byte-wise section of the N-bit wide write data while the other possible data paths for the same respective byte-wise section of the N-bit wide write data are disabled." Micron urges this additional language is necessary because Netlist will otherwise "remove the Court's construction from the context of the claims" and argue, despite express claim language to the contrary, (1) read data paths can satisfy this claim language, Dkt. No. 109 at 11–12 (citing *Samsung I* Trial Tr., Dkt. No. 109-18 at 1373:7–21), and (2) the recited "data path" can be less than a byte, *id.* at 12 (citing *Samsung I* Trial Tr., Dkt. No. 109-18 at 1333:14–21). Netlist frames the disputes similarly—whether "(1) the 'other possible paths' in the Court's prior construction are paths for read data, and (2) the "byte-wise data paths may be a half-byte (i.e., four bits or a nibble) wide." Dkt. No. 112 at 5.

The parties agree the language of Claim 1 is representative of their dispute. Dkt. No. 97 at 9 n.2; Dkt. No. 109 at 10 n.4. The relevant limitations from that claim recite:

> a plurality of byte-wise buffers coupled to the PCB and configured to receive the module control signals, wherein each respective byte-wise buffer of the plurality of byte-wise buffers has a first side configured to be operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple

> N-bit-wide ranks via respective module data lines, and a byte-wise data path between the first side and the second side, wherein the each respective bytewise buffer is disposed on the PCB at a respective position corresponding to the respective set of the plurality of sets of data signal lines;
>
> wherein the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals, wherein the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period; and
>
> wherein the byte-wise data path includes first tristate buffers, and the logic in response to the module control signals is configured to enable the first tristate buffers to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period.

'339 Patent at 19:40–61.

As to the first issue—whether the "other possible paths" in the Court's prior construction can be paths for read data when write data is being "driven"—they cannot. In *Samsung I*, the Court reasoned:

> A skilled artisan would understand "driving" data from one side of the buffer to the other means, when there are multiple paths in a buffer through which *that data* can be driven, enabling only one of the data paths while the other possible paths are disabled. Thus, "to drive" as used in these claims means "enabling only one of the data paths while the other possible paths are disabled."

Cl. Constr. Order, Dkt. No. 97-8 at 10. Netlist's position requires an overly broad interpretation of this reasoning—that "the other possible paths" could pertain to "data" moving the opposite direction from the "driving" direction. "The other possible paths" are paths for the *same data* from

the same "one side of the buffer" to the same "other" side of the buffer. The Court thus agrees with Micron on this first issue.[4]

Regarding the second issue—whether the byte-wise data paths may be a half-byte (i.e., a "nibble") wide—the Court did not previously consider that question. Netlist does not appear to dispute the plain meaning of "byte-wise" refers to a byte rather a nibble. Instead, it points to Figures 3B and 4B as showing byte-wise sections of the N-bit wide data transferred to two 4-bit memory devices rather than one 8-bit memory device. Dkt. No. 97 at 11. This is consistent with the language of Claim 2, which requires the buffers to drive a first and second nibble of the byte-wise section to a pair of DDR DRAM devices). *See id.* at 20:5–13.

Clearly the plain language of the claims requires the respective *data paths* to be at least byte-wise, but that does not prohibit an embodiment in which the memory devices at the end of the data paths might have a less-than-byte-wise width, as shown in Figure 4B and as recited in Claim 2. In other words, while Claim 1's requirement of a byte-wise data path pertains to the electrical connections from the circuits 416, a byte-wise data path can terminate at more than one device. This is consistent with Micron's construction, which the Court adopts: "enable only one of the data paths for the respective byte-wise section of the N-bit wide write data while the other possible data paths for the same respective byte-wise section of the N-bit wide write data are disabled."

[4] Netlist argues the prosecution history supports its position, but only cites to the Court's prior opinion for support without further explanation. *See* Dkt. No. 110 at 5 (citing Dkt. No. 97-8 at 9–10).

VI. U.S. PATENTS 11,016,918 AND 11,232,054

A. Background

These patents concern power management on memory modules. The claimed modules include buck converters—a type of DC-to-DC power converter—that provide power to memory devices. For example, Claim 1 of the '918 Patent recites:

> 1. A memory module comprising:
>
> a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
>
> a first buck converter configured to provide a first regulated voltage having a first voltage amplitude;
>
> a second buck converter configured to provide a second regulated voltage having a second voltage amplitude;
>
> a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;
>
> a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and
>
> a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising:
>
> a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and
>
> at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage,

> wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.

'918 Patent at 38:18–52. Claim 1 of the '054 Patent is similar. *See* '054 Patent at 39:66–40:4 (reciting, in Claim 16, "a voltage conversion circuit [comprising three buck converters] and configured to provide a plurality of voltages").

The Court construed some of the now-disputed terms from these patents in *Samsung I*. Netlist re-urges the constructions adopted by the Court in that proceeding, *see generally* Dkt. No. 97 at 12–18, whereas Micron proposes the construction urged by Samsung and incorporates Samsung's arguments by reference, *see* Dkt. No. 109 at 14. Seeing no new argument by the parties relative to *Samsung I*, the Court adopts its previous reasoning and construction for those terms:

Term	The Court's Construction
"a second plurality of address and control signals" ('918 Patent, Claims 1, 21)	Plain and ordinary meaning
"dual buck converter" ('918 Patent, Claims 2, 17, 28) "dual-buck converter" ('054 Patent, Claim 15)	"a buck converter with two regulated voltage outputs"
"first" / "second" / "third" / "fourth" "regulated voltages"; "first" / "second" / "third" / "fourth" "voltage amplitude" ('918 Patent, Claim 1 and most other claims)	Plain and ordinary meaning
"at least three regulated voltages" ('054 Patent, Claims 1–15)	Plain and ordinary meaning
"a memory module" ('918 Patent, all claims; '054 Patent, all claims)	Limiting

B. "pre-regulated input voltage" / "input voltage" ('918 Patent, Claims 16, 30)

Netlist's Construction	Micron's Construction
plain and ordinary meaning, (i.e., no further construction necessary)	plain and ordinary meaning, where "a pre-regulated input voltage" is different from "an input voltage"

Claim 16 recites "[a] memory module comprising:"

> a printed circuit board (PCB) having an interface . . . including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
>
> first, second, and third buck converters configured to receive *a pre-regulated input voltage* and to produce first, second and third regulated voltages, respectively;
>
> a converter circuit configured to reduce *the pre-regulated input voltage* to provide a fourth regulated voltage, wherein the first, second, third and fourth regulated voltages have first, second, third, and fourth voltage amplitudes, respectively;
>
> . . . ; and
>
> a voltage monitor circuit configured to monitor an *input voltage* received via a first portion of the plurality of edge connections . . . .

'954 Patent at 39:53–40:12 (emphasis added).

"The parties dispute whether the recited 'a pre-regulated voltage' must be different from the separately recited 'an input voltage.'" Dkt. No. 109 at 14. Citing *CAE Screenplates Inc. v. Heinrich Fiedler GmbH & Co. KG*, 224 F.3d 1308, 1317 (Fed. Cir. 2000), Micron argues the separate recitation of these limitations makes clear these terms are different. Dkt. No. 109 at 15. It argues Netlist wrongly interprets the terms so they can be met with a single voltage signal line. *Id.* at 16. Netlist, however, stresses "[t]he claim language requires an 'input voltage' that is 'pre-regulated' to be the input to the conversion circuits, and also describes that the 'input voltage' is

received from 'a first portion of the plurality of edge connections.'" Dkt. No. 110 at 7 (citing '918 Patent at 39:60–62, 40:7–13).

The Court agrees with Netlist. The limitations in which these disputed terms appear are the structural limitations of "buck converters," "a converter circuit" and a "voltage monitor circuit," each of which is configured a certain way. That a buck converter is "configured to receive a pre-regulated input voltage" while the "voltage monitor circuit" is "configured to monitor an input voltage" does not without more exclude the same voltage from being supplied to both structures. Accordingly, the Court rejects Micron's requirement the "pre-regulated input voltage" is different from the "input voltage," and will construe this term to have a "plain and ordinary meaning."

C. "converter circuit" ('918 Patent, all asserted claims)

Netlist's Construction	Micron's Construction
Not subject to § 112, ¶ 6; plain and ordinary meaning, i.e., a circuit for voltage conversion	The "converter circuit" feature is subject to § 112, ¶ 6, with the corresponding functionality being the functions of: (i) "provid[ing] a fourth regulated voltage having a fourth voltage amplitude"; (ii) "reduc[ing] the pre-regulated input voltage to provide a fourth regulated voltage"; (iii) "provid[ing] the fourth regulated voltage"; and (iv) "reduc[ing] the pre-regulated voltage input to provide the fourth regulated voltage". The corresponding structure that is "configured to" perform the recited functions is a "converter circuit," as described in the '918 patent at 29:18–64.

"Converter circuit" appears in Claims 1, 13, 16, 23, and 30 associated with various functions:

Claim 1	a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude
Claim 13	wherein the power input voltage is coupled to the first, second, and third buck converters and the converter circuit
Claim 16	a converter circuit configured to reduce the pre-regulated input voltage to provide a fourth regulated voltage
Claim 23	a converter circuit configured to provide the fourth regulated voltage
Claim 30	a converter circuit configured to provide the fourth regulated voltage [as recited in Claim 23] wherein the converter circuit is configured to reduce the pre-regulated voltage input to provide the fourth regulated voltage

Micron asserts this is a means-plus-function term and stresses the testimony of Netlist's expert during *Samsung I* as evidence this term does not connote sufficiently definite structure. Dkt. No. 109 at 17. Netlist stresses "circuit" is a well-known term in electronics and the prefix "converter" provides structural meaning. Dkt. No. 97 at 19–20.

There is a rebuttable presumption that § 112 ¶ 6 does *not* apply when, as here, the limitation does not use the word "means." See *Masco Corp.*, 303 F.3d at 1326. To rebut that presumption, Micron must show, by a preponderance of the evidence, the limitation fails to recite sufficiently definite structure. *See Dyfan, LLC v. Target Corp.*, 28 F.4th 1360, 1370 (Fed. Cir. 2022) ("In the absence of the word 'means,' Target bore the burden of demonstrating by a preponderance of the evidence that the 'system' limitation in the wherein clause fails to recite sufficiently definite structure.").

Here, in addition to asserting "converter circuit" does not have sufficiently definite structural meaning to a skilled artisan, Micron points to uses of "converter circuit" by Netlist it contends show this is simply a functional term. For example, it points to trial testimony by Netlist's expert in *Samsung I* that "any circuit that converts a voltage is a converter circuit." Dkt. No. 109 at 17 (quoting Trial Tr., Dkt. No. 109-2 at 416:3–5, 416:21–23). Micron also offers its expert's opinion that

> [t]he use of "converter circuit" in the asserted claims provides no guidance of specific structure to a POSITA who would understand the term 'converter circuit' in the asserted claims to be a generic term that encompasses any hardware, software, or combination that may perform the claimed functions of the converter circuit limitation of the asserted claims. In other words, the claim term "converter circuit" does not inform a POSITA of the structural characteristics of the claimed "converter circuit" that is configured to perform the claimed functions of the converter circuit limitation of the asserted claims.

Stone Decl., Dkt. No. 97-9 ¶ 51.

This is not a means-plus-function term. Notably, Dr. Stone does not opine on whether the term "converter circuit" in the abstract has a meaning to a skilled artisan. In other words, his analysis appears limited to "the use of the term 'converter circuit' in the asserted claims." Moreover, two of the dictionaries submitted by Netlist define "converter." *See converter*, Chambers Dict. of Science & Tech., Dkt. No. 97-19 at 274 ("A circuit for changing ac to dc or vice versa. Rating can be a few watts to megawatts."); *converter*, Comprehensive Dict. of Elec. Eng'g, Dkt. No. 97-20 at 148 ("a generic term used in the area of power electronics to describe a rectifier, inverter, or other power electronic device that transforms electrical power from one frequency and voltage to another"). While these definitions are not strictly for the term "converter circuit," given the technical area, they bolster the presumption that § 112 ¶ 6 does not apply. The Court will therefore give this term a "plain and ordinary meaning" construction.

D. "first circuit" ('054 Patent, Claim 1–13, 15)

Netlist's Construction	Micron's Construction
plain and ordinary meaning	"a circuit that is different from a memory module controller"

In the claims, "first circuit" appears only in Claims 1, 21, and 22. In their briefing, the Parties identify the dispute as relating only to Claim 1–13 and 15. Of those claims, only Claims 5 and 7–13 recite a "controller," either directly or through dependance from another claim. '054 Patent at 38:66–39:3 (Claim 5), 39:16–20 (Claim 7), 39:22–29 (Claim 8).

Micron calls its proposal "appropriate" because, without more, "first circuit" does not connote structure. Dkt. No. 109 at 30. Thus, says Micron, a skilled artisan would look to the specification, which describes the "first circuit" as something coupled to SDRAM and the first and second regulated voltages. *Id.* Netlist, however, stresses "memory module controller" does not appear in the specification or claims, and notes Micron has not explained how a "memory module controller" differs from the "controller" recited in the claims. Dkt. No. 97 at 21.

To start, the Court disagrees with Micron's position that "circuit" does not connote structure (or have a plain meaning).[5] *See circuit*, Chambers Dict. of Science & Tech. (2007), Dkt. No. 97-19 at 224 ("An assembly of electronic (or other) components having some specific function, eg amplifier, oscillator or gate"); *circuit*, Comprehensive Dict. of Elec. Eng'g (2005), Dkt. No. 97-20

[5] Whether a term "connotes structure" is normally a means-plus-function dispute, but Micron does not assert this term is governed by § 112 ¶ 6. Rather, Micron appears argue that "circuit" does not have a plain meaning to a skilled artisan so the Court must look to the remainder of the intrinsic record to resolve the term's meaning. *See, e.g.*, *Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1319 (2001) (noting that when a term does not have an ordinary meaning or a meaning clear from a plain reading of the claim, courts turn to the remaining intrinsic evidence, including the written description, to help with construction of the term).

at 112 ("a physical device consisting of an interconnection of elements . . . . For example, an electric circuit may be constructed by interconnecting a resistor and a capacitor to a voltage source."); *circuit*, Dict. of Comput. (2008), Dkt. No. 97-21 at 78 ("The combination of a number of electrical devices and conductors that, when interconnected to form a conducting path, fulfill some desired function").

But assuming Micron's "memory module controller" and the "controller" as recited in the claims are the same, there is a basis for Micron's position that the "first circuit" and "memory module controller" are different things. These claims each recite a "controller" either directly or by dependance on another claim. "Where a claim lists elements separately, 'the clear implication of the claim language' is that those elements are 'distinct component[s]' of the patented invention." *Becton, Dickinson & Co. v. Tyco Healthcare Group*, LP, 616 F.3d 1249, 1254 (Fed. Cir. 2010) (quoting *Gaus v. Conair Corp*., 363 F.3d 1284, 1288 (Fed. Cir. 2004)). The Court will therefore give "first circuit" a "plain and ordinary meaning" while noting the "first circuit" and the recited "controller' are different elements.

E. "at least one circuit" ('918 Patent, Claims 1, 21)

Netlist's Construction	Micron's Construction
Not subject to § 112(6); plain and ordinary meaning. If subject to §112(6), then: Function: (i) receive a first plurality of address and control signals via [the first/a second] portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices. Structures: As described in 21:14-23, 23:27-31, 23:41-24:8 or equivalents thereof.	The "at least one circuit" feature is subject to §112, ¶ 6, with the corresponding functionality being the functions of: (i) "receiv[ing] a first plurality of address and control signals via the first portion of the plurality of edge connections"; (ii) "output[ting] a second plurality of address and control signals to the plurality of SDRAM devices"; (iii) "receiv[ing] a first plurality of address and control signals via a second portion of the plurality of edge connections"; and (iv) "output a second plurality of address and control signals to the plurality of SDRAM devices". The corresponding structure that is "operable to" perform the recited functions is a "circuit that is different from a memory module controller," as described in the '918 patent at 21:14–26:65, 29:33–54.

This term is found in nearly identical limitations in Claim 1 and Claim 21. The former recites:

> *at least one circuit* coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.

'918 Patent at 38:41–52 (emphasis added). Similarly, Claim 21 recites:

> *at least one circuit* coupled between the interface and the plurality of SDRAM devices, the at least one circuit operable to receive a first plurality of address and control signals via a second portion of the plurality of edge connections and to output a second plurality of address and control signals to the plurality of SDRAM devices, the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.

Id. at 40:31–42 (emphasis added).

Micron contends these are means-plus-function terms for three reasons.[6] First, the format of the limitations is consistent with traditional means-plus-function claiming. Dkt. No. 109 at 21. Second, "circuit" is a generic nonce term that does not provide any indication of structure. *Id.* at 21–22. Third, the remaining claim language fails to describe any structure for performing the claimed function. *Id.* at 22.

For a limitation that does not use the word "means," the party asserting § 112(6) bears the burden of showing, by a preponderance of the evidence, the limitation fails to recite sufficiently definite structure. *See Dyfan*, 28 F.4th at 1370 ("In the absence of the word 'means,' Target bore the burden of demonstrating by a preponderance of the evidence that the 'system' limitation in the wherein clause fails to recite sufficiently definite structure.").

Here, Micron proffers its expert's opinion that "[t]he use of 'at least one circuit' in [the claims] provides no guidance of specific structure to a POSITA who would understand the term

[6] Based on Micron's proposed "corresponding structure" for this term, its goal seems to be clarifying that the "at least one circuit" is different from the "memory module controller" in line with its proposed construction for "first circuit" in the '054 Patent.

'at least one circuit.'" Stone Decl., Dkt. No. 97-9 ¶ 55. And "the remaining claim language specifies merely additional functions that the claimed 'at least one circuit' be configured to perform." *Id.* ¶ 56. But Stone provides no analysis of how a skilled artisan would interpret what he calls the "additional functions," or why the "additional functions" would not convey sufficient additional structure to a skilled artisan. *See id.*

"When the structure-connoting term 'circuit' is coupled with a description of the circuit's operation, sufficient structural meaning generally will be conveyed to persons of ordinary skill in the art, and § 112 P 6 presumptively will not apply." *Linear Tech. Corp. v. Impala Linear Corp.*, 379 F.3d 1311, 1320 (Fed. Cir. 2004). Here, the claim language suggests additional structure. A skilled artisan would at least understand the "at least one circuit" includes the structure to receive and transmit address and control lines. Moreover, the "at least one circuit" must have the structure to accept the second and fourth regulated voltages. Yet Stone does not address these aspects of the limitation's language with any specificity and fails to explain why this structure would not be known to a skilled artisan. The Court thus concludes Micron has not shown, by a preponderance of the evidence, the limitation fails to connote sufficiently definite structure.

F. "controller" ('918 Patent, Claims 12, 18–19, 25–26; '054 Patent, Claims 5, 7–13, 16–17, 23–25, 29–30)

Netlist's Construction	Not subject to § 112(6) and not indefinite; plain and ordinary meaning. To the extent that "controller" is a § 112(6) term, the function and corresponding structure vary for each claim, contrary to Micron's attempt to aggregate all functions into the term. Structures: ASIC, PLD, CPLD, FPGA, custom- designed semiconductor device as described in 23:1–27, 24:35–37, 25:8–31, 29:33–54, 32:49–51 or equivalents thereof.
Micron's Construction	**'918 Patent** The "controller" feature is subject to § 112, ¶ 6, with the corresponding functionality being the functions of: (i) "receiv[ing] the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory"; (ii) "receiv[ing] the signal, wherein the controller executes a write operation in response to the signal"; and (iii) "receiv[ing] the signal, wherein, in response to the signal, the controller executes a write operation". The corresponding structure that is "configured to" perform the recited functions is a "controller that is different from the at least one circuit and the voltage monitor circuit and the one or more registers," as described in the '918 patent at 21:14–26:65, 29:33–54. **'054 Patent** The "controller" feature is subject to § 112, ¶ 6, with the corresponding functionality being the functions of: (i) "perform[ing] one or more operations including a write operation to transfer data to non-volatile memory" "in response to the trigger signal"; and (ii) "perform[ing] one or more operations in response to the voltage monitor circuit detecting an amplitude change in the input voltage, and wherein the one or more operations include a write operation to transfer data into non-volatile memory." The corresponding structure that is "configured to" perform the recited functions is a "controller that is different from the first circuit and the voltage monitor circuit," as described in the '054 patent at 21:14–26:65, 29:33–54.

The "controller" limitations are recited various ways. Some claims recite "a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory." '918 Patent at 39:34–36 (Claim 12); *see also id.* at 42:3–5 (reciting, in Claim 25, "a controller coupled to the voltage monitor circuit; wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory"). Other claims recite:

> a controller coupled to the PCB, the controller including a voltage monitor circuit configured to monitor an input voltage received from a second set of edge connections of the plurality of edge connections, wherein, in response to the voltage monitor circuit detecting a power threshold condition, the voltage monitor circuit transmits a signal to one or more portions of the controller.

'054 Patent at 39:22–29 (Claim 8); *see also id.* at 40:13–20 (Claim 16)

Asserting this is a means-plus-function term, Micron makes similar arguments to those it made with respect to "at least one circuit": (1) the various forms of the limitations are consistent with traditional means-plus-function claiming; (2) "controller" is a nonce term that does not provide any indication of structure; and (3) the remaining claim language fails to describe any structure for performing the claimed function. Dkt. No. 109 at 22. For support, Micron proffers its expert's opinion that:

> The use of "controller" in th[e] claims provides no guidance of specific structure to a POSITA who would understand the term "controller" . . . to be a generic term that encompasses any hardware, software, or combination that may perform the claimed functions of the controller limitation . . . . In other words, the claim term "controller" does not inform a POSITA of the structural characteristics of the claimed "controller" that is configured to perform the claimed functions . . . . of the controller limitation of claims 12,

> 18–19, and 25–26 of the '918 patent and claims 5, 7–13, 16–17, 23–25, and 29–30 of the '054 patent.
>
> . . . the remaining claim language specifies merely additional functions that the claimed "controller" be configured to perform. None of this language . . . provides any indication of a structure or category of structures narrowing the understanding of a POSITA that any hardware, software, or combination could be used to perform the claimed functions of the controller limitation.

Stone Decl., Dkt. No. 97-9 ¶¶ 59–60.

This is not a means-plus-function term. For one, Micron's arguments about "controller" being a nonce term are not persuasive. "Controller" in the context of this patent clearly connotes a well-known class of structures. Micron points to *Incom Corp. v Radiant RFID, LLC*, No. 1-17-CV-009-LY, 2018 WL 4690934 (W.D. Tex. Sept. 28, 2018), for support, but *Incom*'s patent did not concern the electronic arts. Instead, the relevant claim recited "a tag orientation controller adapted to keep [a remotely readable] tag with its length extending substantially horizontally and extending lateral to the human user when said tag suspension is in use coupling the tag to the human user[.]." U.S. Patent 7,336,185 at 5:37–40. Because, in part, the phrase "tag orientation controller" did not appear in the specification, the court ultimately construed the term as a means-plus-function term with the corresponding structure as "a tag container snugly held within a second pouch of the holder." *Incom*, 2018 WL 4690934, *6. Micron's reliance on *Incom* is questionable given the disparate levels of skill applicable to the two patents and the obviously different contexts in which "controller" is used.

Moreover, as with his opinion regarding "at least one circuit," Dr. Stone fails to explain why the "additional functions" would not convey sufficient additional structure to a skilled artisan. *Linear Tech. Corp.*, 379 F.3d at 1320) ("when the structure-connoting term 'circuit' is coupled with

a description of the circuit's operation, sufficient structural meaning generally will be conveyed to persons of ordinary skill in the art, and § 112 P 6 presumptively will not apply"). He simply concludes that to be the case. Accordingly, the Court concludes Micron has not shown, by a preponderance of the evidence, the limitation fails to recite sufficiently definite structure and will give this term a "plain and ordinary meaning" construction.

G. "first operable state" and "second operable state" ('054 Patent, Claims 4–7, 11–12, 16–17, 23, 25)

Netlist's Construction	Micron's Construction
"first operable state" is a "state in which the memory module is operated before transition"	"state in which a controller and a non-volatile memory subsystem are operatively decoupled (e.g., isolated) from a volatile memory subsystem by at least one circuit," or in the alternative, indefinite
"second operable state" is a "state in which the memory module is operated after transition"	"state in which the volatile memory subsystem is operatively coupled to the controller to allow data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem via the controller," or in the alternative, indefinite

Generally, these terms appear in limitations requiring the transition of the memory module from a "first operable state" to a "second operable state" in response to some transition signal. *See, e.g.*, '054 Patent at 38:62–64 (reciting, in Claim 4, "wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal"). The specification never uses the phrases "first *operable* state" or "second *operable* state," but does use the phrases "first state" and "second state":

> The memory system 1010 of certain embodiments is configured to be operated in at least two states. The at least two states can comprise a *first state* in which the controller 1062 and the non-volatile memory subsystem 1040 are operatively decoupled (e.g., isolated) from the volatile memory subsystem 1030 by the at least

> one circuit 1052 and a *second state* in which the volatile memory subsystem 1030 is operatively coupled to the controller 1062 to allow data to be communicated between the volatile memory subsystem 1030 and the nonvolatile memory subsystem 1040 via the controller 1062. The memory system 1010 may transition from the *first state* to the *second state* in response to a trigger condition, such as when the memory system 1010 detects that there is a power interruption (e.g., power failure or reduction) or a system hang-up.

'054 Patent at 24:60–25:7 (emphasis added). Micron stresses "[t]here is no other disclosure that describes what is meant when the claims recite that a 'memory module' 'transitions' from a 'first operable state' to a 'second operable state' 'in response to" some trigger associated with the 'input voltage.'" Dkt. No. 109 at 29. Thus, argues Micron, if the disputed terms do not mean this, they must be indefinite.

In Netlist's view, Micron's position improperly limits "operable state" to a specific embodiment. Dkt. No. 97 at 29. Netlist also accuses Micron of confusing breadth with indefiniteness. *Id.* at 30.

The Court agrees with Netlist. The Court sees no lexicography, which is essentially what Micron seeks. Even assuming that the "operable states" of the claims are the first and second states of the specification, the surrounding claim language and nature of the terms is sufficient to avoid limiting the terms to the specific states mentioned in the specification. Regarding Micron's alternative "indefiniteness" position, it only argues there are no bounds to the claim. That, however, presumes a skilled artisan both would not understand the meaning of "operable state" in the context of the disclosure. Micron proffers no evidence on that point, and thus cannot carry its clear-and-convincing burden. Accordingly, the Court adopts Netlist's construction for these terms and construes "first operable state" as "state in which the memory module is operated before transition" and "second operable state" as "state in which the memory module is operated after transition."

VII. CONCLUSION

Term	The Court's Construction
"electrical communication" ('060 Patent, Claims 1, 11, 20, 29; '160 Patent, Claim 1)	Plain and ordinary meaning
"driver size" ('160 Claim 1)	"driver physical size"
Claim 7 ('060 Patent)	Not indefinite as a mixed-class claim
"one or more previous operations" ('506 Patent, Claims 1–3, 11, 15, 16)	"one or more previous memory operations"
"determining" ('506 Patent, Claim 14)	Plain and ordinary meaning
"to actively drive a respective byte-wise section of the N-bit wide write data" ('339 Patent, Claim 1) "to actively drive a respective section of the N-bit wide write data" ('339 Patent, Claim 11) "to actively drive a respective section of the [first/second] N-bit wide data" ('339 Patent, Claim 19) "to drive the respective n-bit section of the write data" ('339 Patent, Claim 27)	"to enable only one of the data paths for the respective byte-wise section of the N-bit wide write data while the other possible data paths for the same respective byte-wise section of the N-bit wide write data are disabled"
"a second plurality of address and control signals" ('918 Patent, Claims 1–3, 4-7, 9–13, 15, 21)	Plain and ordinary meaning

Term	The Court's Construction
"dual buck converter" ('918 Patent, Claims 2, 17, 28) "dual-buck converter" ('054 Patent, Claim 15)	"a buck converter with two regulated voltage outputs"
"first" / "second" / "third" / "fourth" "regulated voltage"; "first" / "second" / "third" / "fourth" "voltage amplitude" ('918 Patent, all asserted Claims)	Plain and ordinary meaning
"at least three regulated voltages" ('054, Claims. 1, 16, 24)	Plain and ordinary meaning
"a memory module" ('918 Patent, all Claims; '054 Patent, all Claims)	Limiting
"pre-regulated input voltage" / "input voltage" ('918 Patent, Claims 16, 30)	Plain and ordinary meaning
"converter circuit" ('918 Patent, all asserted claims)	Plain and ordinary meaning Not governed by 35 U.S.C. § 112 ¶ 6
"first circuit" ('054 Patent, Claim 1–13, 15)	Plain and ordinary meaning
"at least one circuit" ('918, Claims 1–3, 5-7, 9–13, 15, 21)	Plain and ordinary meaning Not governed by 35 U.S.C. § 112 ¶ 6
"controller" ('918, Claims. 12,18–19, 25–26; '054 Patent, Claims 5,7–13, 16–17, 23–25, 29–30)	Plain and ordinary meaning Not governed by 35 U.S.C. § 112 ¶ 6
"first operable state" and "second operable state" ('054 Patent, Claims 4–7, 11–12, 16–17, 23, 25)	**"first operable state":** "state in which the memory module is operated before transition" **"second operable state":** "state in which the memory module is operated after transition"

The Court **ORDERS** each party not to refer, directly or indirectly, to its own or any other party's claim-construction positions in the presence of the jury. Likewise, the Court **ORDERS** the

parties to refrain from mentioning any part of this opinion, other than the actual positions adopted by the Court, in the presence of the jury. Neither party may take a position before the jury that contradicts the Court's reasoning in this opinion. Any reference to claim construction proceedings is limited to informing the jury of the positions adopted by the Court.

SIGNED this 21st day of October, 2023.

ROY S. PAYNE
UNITED STATES MAGISTRATE JUDGE